Techniques in Hardware Verification

Verification of Complex Parallel Systems

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Contents

- Design validation approaches

- Used methods in verification of complex systems

    - modular way

    - symmetry

    - abstractions

- Formal verification in practice

- Conclusion and summary of my study

Design Validation

- Simulation

  - simple modeling, fast process

- Testing

- Formal verification

  - exhaustive state space exploration

  - state space explosion problem

  - small set of applications

Methods to the State Explosion Problem

- Partial Order Reduction

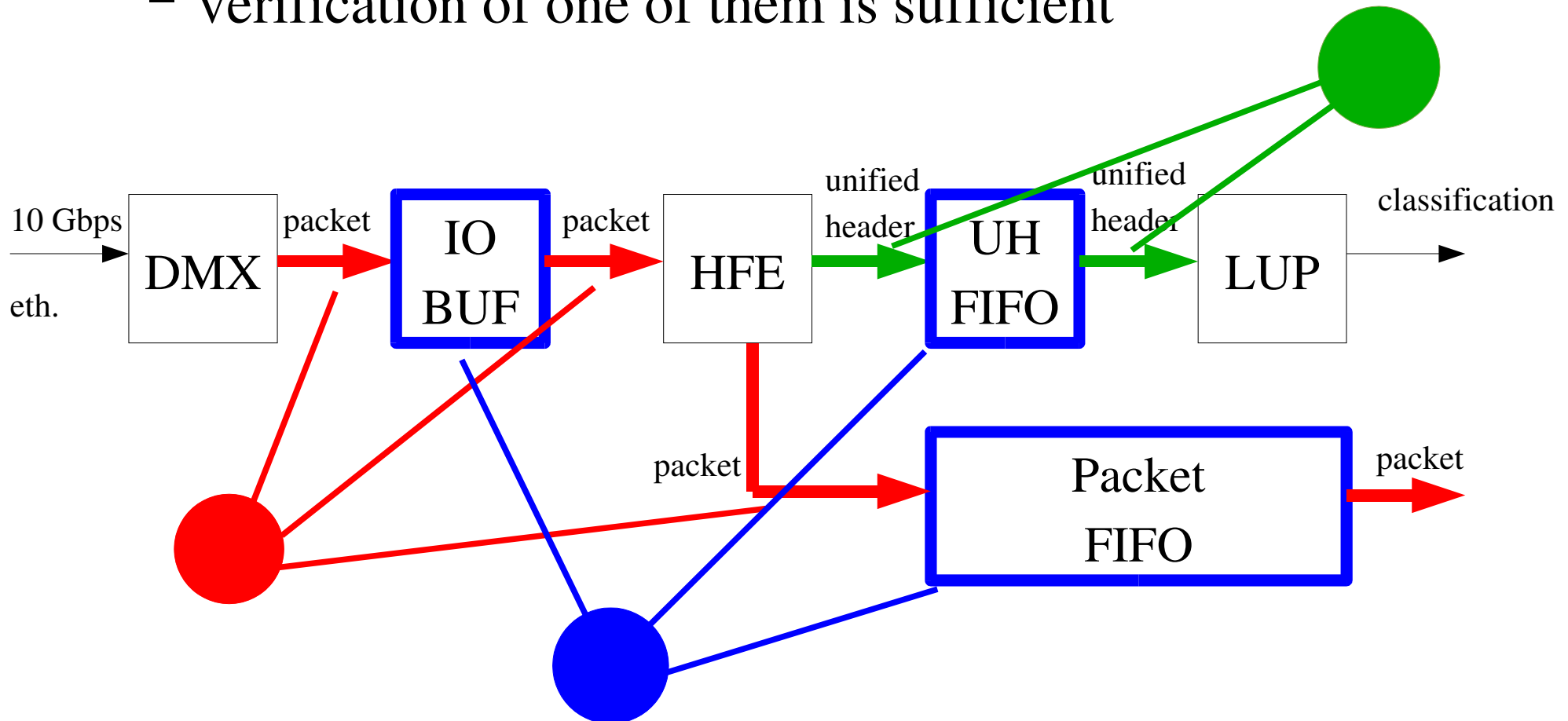- Compositional reasoning

- Symmetry

- Abstractions

- Induction

Compositional Reasoning

- Verification of small components
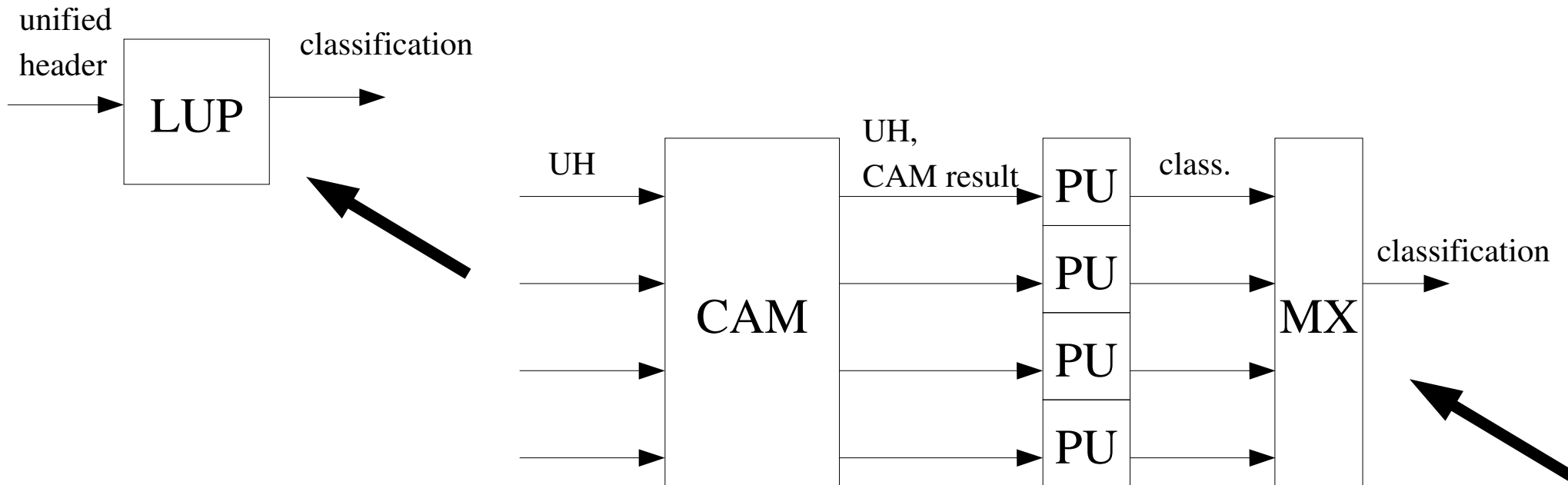
- Verification of communication protocols
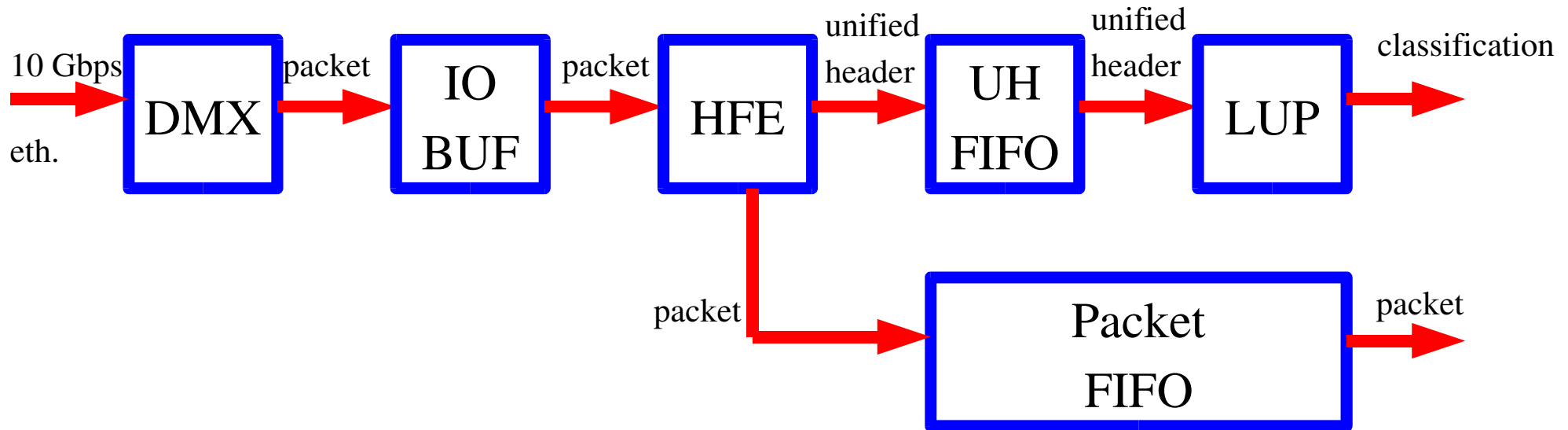
Symmetry reduction

- Finding replicated components
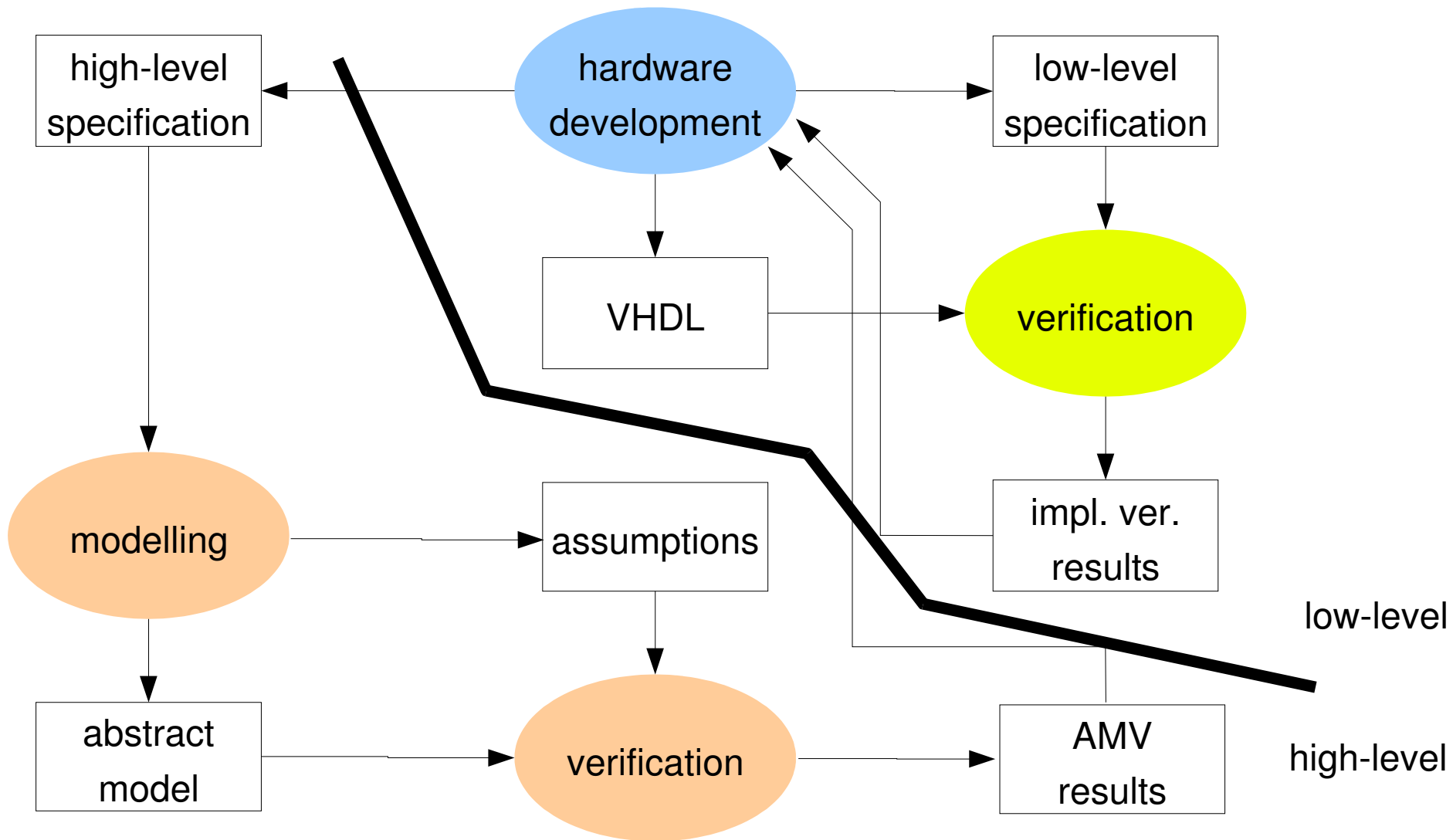 - verification of one of them is sufficient

Abstractions

- State Merging Abstraction

- Variable Abstraction (Data Abstraction)

- Abstraction by Limitation

Formal Verification within Liberouter

Conclusion

- First practical experiences

  - abstract model verification of the lookup processor

- Thesis motivated by real cases

  - automatic abstractions

  - automatic symmetry

Annual Review

- Teaching:
  - IZP & IUS (projects) + IAS (Czech and foreign students)
  - 2 projects (Web Framework and File-system Guard)
- Publications:
  - A. Smrčka. *Towards Hardware Verification.* EEICT
  - A. Smrčka. *Abstract Model Verification of LUP.* MOSIS
  - P. Matoušek, A. Smrčka, T. Vojnar. *High-level Modelling, Analysis and Verification on FPGA-based Hardware Design.* CHARME submitted